

IN THE CLAIMS:

The claims are amended as follows:

1 1. (Currently Amended) ~~An integrated~~A circuit ~~with a~~for jitter measurement circuit, comprising:
2 a plurality of delay elements, ~~each delay element having an associated delay, an input~~
3 ~~configured to receive an input clock signal and an output responsive to the associated delay and~~
4 ~~the input clock signal, wherein the input clock signal has a significant instant; arranged in a~~
5 ~~series-connected chain having a total delay equal to the sum of the delays of the delay elements,~~
6 ~~wherein the first element in the chain has an input that receives an input clock signal, the chain~~
7 ~~propagating the input clock signal through each of its elements, and each delay element output~~
8 ~~producing a delayed version of the signal on its input;~~
9 ~~— a first set of circuitry connected to the inputs and outputs of the plurality of delay~~
10 ~~elements, said first set of circuitry configured to detect the significant instant on the input clock~~
11 ~~signal, the first set of circuitry further configured to output a signal responsive to the significant~~
12 ~~instant on the input clock signal; and~~
13 a first set of circuitry operative to produce at an output a pulse corresponding to each
14 delay element in response to the propagation of a significant instant of the input clock signal
15 through the delay element, each pulse having a width that is approximately equal to the delay of
16 the corresponding delay element; and
17 a second set of circuitry ~~configured to receive the signal responsive to the significant~~
18 ~~instant on the input clock signal and a first~~having one storage element corresponding to each
19 output of the first set of circuitry, and an input that receives a trigger signal, that is timed to
20 correspond to a delay which is approximately half of the total delay of the chain, and
21 ~~the second set of circuitry further configured to latch onto the signal responsive to the significant~~
22 ~~instant on the input clock signal and further responsive to a significant instant on the first trigger~~
23 ~~signal, wherein a measure for jitter is determined from the latched signal responsive to the~~
24 ~~significant instant on the input clock signal; being operative to record in the corresponding~~
25 storage element any pulse that is active at the time of occurrence of the trigger signal, wherein a
26 jitter measurement is made based on the pulses recorded in the storage elements after a plurality
27 of trigger signals has occurred.

1 2. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the output of one
2 delay element is connected to the input of the next adjacent delay element~~associated delay of~~
3 ~~each delay element is approximately equal.~~

1 3. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the number of delay
2 elements in the chain is N, where N is an even number greater than 2 and implemented as a
3 power of 2~~the plurality of delay elements are serially connected together.~~

1 4. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the associated delay of
2 each delay element is controlled by a delay control circuit.

1 5. (Currently Amended) The ~~integrated~~ circuit of claim 4, wherein at least one of the
2 plurality of associated delays is not equal to any other of the plurality of associated delays, and
3 wherein the delay control circuit is a charge pump controlled delay lock loop.

1 6. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the first set of circuitry
2 includes a plurality of two-input logic gates, with each of the plurality of two-input logic gates
3 corresponding to ~~each~~ a respective one of the plurality of delay elements.

1 7. (Currently Amended) The ~~integrated~~ circuit of claim 6, wherein ~~the inputs~~ each of the
2 plurality of two-input logic gates is coupled to the input and the output of a corresponding one
3 of the plurality of delay elements.

1 8. (Currently Amended) The ~~integrated~~ circuit of claim 7, wherein one of ~~the~~ the two
2 inputs of each of the plurality of two-input logic gates ~~gate~~ is coupled to the output of its
3 corresponding delay element ~~by means of~~ via an inverter logic gate.

1 9. (Currently Amended) The ~~integrated~~ circuit of claim 7, wherein one of the two inputs
2 of each of ~~the plurality of~~ two-input logic gates is coupled to the output of its corresponding
3 delay element by means of wired connection.

1 10. (Currently Amended) The ~~integrated~~ circuit of claim 6, wherein each of the plurality of
2 two-input logic gates is capable of producing a pulse with a width approximately equal to the
3 delay of its corresponding delay elements~~signal responsive to the significant instant on the input~~
4 ~~clock signal.~~

1 11. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the second set of
2 circuitry includes a first plurality of latching circuits each, ~~each of the first plurality of~~
3 ~~latching circuits~~ corresponding to each one of the plurality of delay elements.

1 12. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the input clock signal
2 is related to a reference clock signal.

1 13. (Currently Amended) The ~~integrated~~ circuit of claim 12, wherein the trigger signal is
2 delayed by a first predetermined delay from the reference clock signal.

1 14. Cancelled.

1 15. (Currently Amended) The ~~integrated~~ circuit of claim 13, wherein a measure ~~for~~ of jitter
2 is determined by comparing ~~the a latched signal responsive to the significant instant on the~~
3 ~~input clock signal~~ pulse to the first predetermined delay.

1 16. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein the measure ~~for~~ of
2 jitter is filtered.

1 17. (Currently Amended) The ~~integrated~~ circuit of claim ~~16~~ 1, wherein the second set of
2 circuitry further includes a single one detector for filtering the measure of jitter ~~is filtered by~~
3 ~~means of a single one detector.~~

1 18. (Currently Amended) The ~~integrated~~ circuit of claim 1, wherein ~~the latched pulses are~~
2 ~~signal responsive to the significant instant on the input clock signal~~ is recorded for a first
3 number of significant instants ~~on~~ of the first trigger signal.

1 19. (Currently Amended) The ~~integrated~~ circuit of claim ~~18~~1, further comprising a third
2 set of circuitry for recording pulses ~~wherein the latched signal responsive to the significant~~
3 ~~instant on the input clock signal is recorded by a third set of circuitry.~~

1 20. (Currently Amended) The ~~integrated~~ circuit of claim 19, wherein the third set of
2 circuitry includes a second plurality of latching circuits; ~~each of the second plurality of~~
3 ~~latching circuits~~ corresponding to ~~each one of~~ the plurality of delay elements.

1 21. (Currently Amended) The ~~integrated~~ circuit of claim 20, wherein each of the second
2 plurality of latching circuits is provided with logic circuitry in a feedback loop for recording
3 the presence of a desired input to the second plurality of latching circuits.

1 22. (Currently Amended) The ~~integrated~~ circuit of claim 21, wherein the desired input to
2 the second plurality of latching circuits is a logic level high.

1 23. (Currently Amended) The ~~integrated~~ circuit of claim 1, further comprising a result
2 calculator configured to provide information collected from the measure of jitter.

1 24. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising
2 wherein the result calculator connected to the second plurality of latching circuits and is
3 ~~configured to provide for receiving recorded pulses and based thereon providing information~~
4 ~~of on an earliest occurrence in the chain of the significant instant on of the propagating input~~
5 ~~clock signal.~~

1 25. (Currently Amended) The ~~integrated~~ circuit of claim ~~23~~19, further comprising
2 wherein the result calculator connected to the second plurality of latching circuits and is
3 ~~configured to provide for receiving recorded pulses and based thereon providing information~~
4 ~~of on a latest occurrence in the chain of the significant instant on of the propagating input~~
5 ~~clock signal.~~

1 26. (Currently Amended) The ~~integrated~~ circuit of claim 2319, further comprising
2 ~~awherein the result calculator connected to the second plurality of latching circuits and is~~
3 ~~configured to provide for receiving recorded pulses and based thereon providing information of~~
4 ~~on a difference between an earliest and a latest occurrence in the chain of the significant~~
5 ~~instant on of the propagating input clock signal.~~

1 27. (Currently Amended) The ~~integrated~~ circuit of claim 2319, further comprising
2 ~~awherein the result calculator connected to the second plurality of latching circuits and is~~
3 ~~configured to provide for receiving recorded pulses and based thereon providing median or~~
4 ~~average information on the occurrences an average of the significant instant on of the input~~
5 ~~clock signal.~~

1 28. Cancelled.

1 29. (Currently Amended) The ~~integrated~~ circuit of claim 2319, further comprising
2 ~~awherein the result calculator connected to the second plurality of latching circuits and is~~
3 ~~configured to provide for receiving recorded pulses and based thereon providing information~~
4 ~~on a standard deviation of in the occurrences of the significant instant on of the input clock~~
5 ~~signal.~~

1 30. (Currently Amended) The ~~integrated~~ circuit of claim 23, wherein the result calculator
2 is configured to provide information responsive to a mode selection signal.

1
2 31.— (Currently Amended) A method for measuring jitter of a ~~significant instant on a clock~~
3 ~~signal derived from a reference clock signal~~, comprising:

4 _____ for each of a plurality of trigger signal occurrences, performing the steps of

5 _____ receiving an input the clock signal, wherein the input clock signal

6 ~~has~~ having a significant instant; _____

7 propagating the significant instant; delaying of the input clock signal

8 by through a first chain of delay elements, wherein each element has an associated delay

9 and the chain has a total delay equal to produce a delayed input clock signal and a

10 ~~delayed significant instant on the delayed input clock signal~~the sum of the associated
11 delays;
12 _____ receiving a trigger signal, wherein and delaying the received trigger signal is
13 delayed from the reference clock signal by to occur at a second time equal to approximately
14 half the total delay; detecting of the delayed significant instant on the delayed input clock
15 signal; and chain;
16 _____ detecting propagation of the significant instant of the clock signal through each of
17 the delay elements in the chain and producing a pulse corresponding thereto;
18 _____ recording any pulse that is coincident with the trigger signal; and
19 _____ producing a jitter measurement signal responsive to the delayed significant instant
20 on the delayed input clock signal and the trigger signal. recorded pulses after the plurality of
21 trigger signal occurrences.

1 32. (Currently Amended) The method of claim 31, further comprising deriving a jitter
2 measure through a comparison of the jitter measurement signal to ~~the~~ an associated first delay.

1 33. (Currently Amended) The method of claim 31, further comprising filtering the jitter
2 measurement signal to produce a filtered jitter measurement signal.

1 34. (Currently Amended) The method of claim 33, wherein the filtered jitter measurement
2 signal contains information of an earliest occurrence in the chain of the ~~delayed propagating~~
3 significant instant ~~on~~ of the ~~delayed~~ input clock signal.

1 35. (Currently Amended) The method of claim 33, wherein the filtered jitter measurement
2 signal contains information of a latest occurrence in the chain of the ~~delayed~~
3 propagating significant instant ~~on~~ of the ~~delayed~~ input clock signal.

1 36. Cancelled.

1 37. (Currently Amended) The method of claim 36, further comprising determining an
2 earliest occurrence in the chain of the propagating significant instant.

1 38. (Currently Amended) The method of claim 36, further comprising determining a latest
2 occurrence in the chain of the propagating significant instant ~~on the delayed input clock signal~~.

1 39. (Currently Amended) The method of claim 36, further comprising determining a
2 difference between an earliest and latest occurrence in the chain of the propagating significant
3 instant ~~on the delayed input clock signal~~.

1 40. (Currently Amended) The method of claim 36, further comprising determining a
2 statistical information on the occurrences in the chain of the propagating significant instant ~~on~~
3 ~~the delayed input clock signal~~.

1 41. (Currently Amended) The method of claim 31, wherein an associated frequency of the
2 reference clock signal is adjusted ~~responsive~~ in response to the jitter measurement signal.

1 42. (Currently Amended) The method of claim 31, wherein the ~~first-trigger~~ delay is
2 adjusted ~~responsive~~ in response to the jitter measurement signal.

1 43. (Currently Amended) The method of claim 31, further comprising receiving a reset
2 signal, wherein the reset signal is delayed by a second delay relative to the reference clock
3 signal which is adjusted ~~responsive~~ in accordance with the jitter measurement signal.

1 44. (Currently Amended) The method of claim 31, further comprising inputting the
2 reference clock signal to a circuit to produce the input clock signal.

1 45. (Currently Amended) The method of claim 44, wherein the circuit is adjusted
2 ~~responsive~~ in accordance with the jitter measurement signal.

1 46. (Currently Amended) A system for responding ~~responsive~~ to jitter ~~in the~~
2 ~~system~~ therein, comprising:
3 a reference clock configured to generate a reference clock signal having an associated

4 frequency;
5 a plurality of circuits configured to receive the reference clock signal and operative to
6 generate an input clock signal, the plurality of circuits having a first set of characteristics; and
7 a jitter measurement sub-system configured to receive the reference clock signal and the
8 input clock signal and operative to generate a jitter measurement output signal responsive to a
9 significant instant of the input clock signal, wherein the jitter measurement sub-system
10 includes:
11 a plurality of delay elements having a plurality of associated delays configured to
12 generate a synthesized signal from the reference clock signal and the input clock signal; and
13 at least one programmable delay element having at least one associated
14 programmable delay configured to produce a trigger signal for generating the jitter
15 measurement output signal from the synthesized signal;
16 wherein the system is operative to adjust at least one parameter of the system
17 ~~responsive in accordance with~~ the jitter measurement output signal.

1 47. (Original) The system of claim 46, wherein the at least one parameter of the system is
2 at least one parameter of the jitter measurement sub-system.

1 48. (Original) The system of claim 46, wherein the at least one parameter includes the
2 associated frequency.

1 49. (Original) The system of claim 46, wherein the reference clock signal further has an
2 associated duty cycle, and the at least one parameter includes the associated duty cycle.

1 50. (Original) The system of claim 46, wherein the at least one parameter includes at least
2 one characteristic from the first set of characteristics.

1 51. (Currently Amended) The system of claim 46, wherein the plurality of circuits
2 includes a plurality of sub-circuits having a second set of characteristics, and wherein the at
3 least one parameter includes at least one characteristic from the second set of characteristics.

1 52. (Currently Amended) The system of claim 46, wherein the output of one delay element
2 is connected to the input of the next adjacent delay element~~each of the plurality of associated~~
3 ~~delays is equal.~~

1 53. (Currently Amended) The system of claim 46, wherein at least one of the plurality of
2 associated delays is not equal to any other of the plurality of associated delays.

1 54. (Original) The system of claim 46, wherein the at least one parameter includes at least
2 one of the plurality of associated delays.

1 55. (Original) The system of claim 46, wherein the at least one parameter includes all of
2 the plurality of associated delays.

1 56. (Original) The system of claim 46, wherein the at least one parameter includes the at
2 least one associated programmable delay.

1 57. (New) A jitter measurement circuit comprising:

2 a plurality of delay elements arranged in a series-connected chain having a total delay
3 equal to the sum of the delays of the delay elements, wherein the first element in the chain has an
4 input that receives an input clock signal, the chain propagating the input clock signal through
5 each of its elements, and each delay element output producing a delayed version of the signal on
6 its input;

7 a first set of circuitry operative to produce at an output a pulse corresponding to each
8 delay element in response to the propagation of a significant instant of the input clock signal
9 through the delay element, each pulse having a width that is approximately equal to the delay of
10 the corresponding delay element; and

11 a second set of circuitry having one storage element corresponding to each output of the
12 first set of circuitry, and an input that receives a trigger signal that is timed to correspond to a
13 delay which is approximately half of the total delay of the chain, and the second set of circuitry
14 being operative to record in the corresponding storage element any pulse that is active at the time
15 of occurrence of the trigger signal, wherein a jitter measurement is made based on the pulses

16 recorded in the storage elements after a plurality of trigger signals has occurred.

1 58. (New) A circuit for jitter analysis as in claim 57, further comprising:
2 a single one detector for receiving a reset signal and for filtering the measure of jitter
3 by selecting one instance of the recoded pulses in response to occurrence of the reset signal;
4 and
5 a result calculator for producing statistical information about occurrences in the chain
6 of the significant instance of the input clock signal.